layers formed upon a second of the three semiconductor substrates was formed an undoped silicate glass (USG) (i.e. silicon oxide) layer employing materials and deposition conditions equivalent to the materials and deposition conditions employed for forming the fluorosilicate glass (FSG) low dielectric constant dielectric layer over the first of the three semiconductor substrates, but where there was not employed a flow of the silicon tetrafluoride fluorine source material.

Upon a third of the three patterned conductor layers formed upon a third of the three silicon oxide dielectric layers formed upon a third of the three semiconductor substrates was formed a fluorosilicate glass (FSG) low dielectric constant dielectric layer as is more conventional in the art of microelectronic fabrication. The fluorosilicate glass (FSG) low dielectric constant dielectric layer was formed employing materials and process conditions otherwise equivalent to the materials and process conditions employed for forming the fluorosilicate glass (FSG) low dielectric constant dielectric layer upon the first of the three patterned conductor layers formed upon the first of the three silicon oxide dielectric layers formed upon the first of the three silicon semiconductor substrates, but wherein the silicon semiconductor substrate temperature was about 450 degrees centigrade as controlled by a backside helium pressure of about 2.5 torr.

Each of the two fluorosilicate glass (FSG) low dielectric constant dielectric layers and the undoped silicate glass (USG) dielectric layer were then chemical mechanical polish (CMP) planarized without exposing each of the three series of patterned conductor lines within the three patterned conductor layers.

There was then measured the line-to-line capacitances of adjoining lines within the three patterned conductor layers while employing electrical measurement methods as are conventional in the art of microelectronics fabrication. The data so obtained for each individual patterned conductor layer was plotted as cumulative percentage versus line-to-line capacitance, as illustrated within FIG. **3**.

As shown within FIG. **3**, the data points corresponding with reference number **30** correspond with the fluorosilicate glass (FSG) low dielectric constant dielectric layer formed over the third silicon semiconductor substrate at the silicon semiconductor substrate temperature of about 450 degrees centigrade corresponding with the backside helium pressure of about 2.5 torr. Similarly, the data points corresponding with reference number **32** correspond with the fluorosilicate glass (FSG) low dielectric constant dielectric layer formed in accord with the preferred embodiment of the present invention upon the first silicon semiconductor substrate at the semiconductor substrate temperature of about 410 degrees centigrade corresponding with the backside helium pressure of about 4 torr. Finally, the data points corresponding with reference numeral **34** correspond with the undoped silicate glass (USG) (i.e. silicon oxide) dielectric layer formed upon the second silicon semiconductor substrate at the silicon semiconductor substrate temperature of about 410 degrees centigrade corresponding with the backside helium pressure of about 4 torr.

Within FIG. **3**, a more vertical character of a line approximating a pertinent series of data points is indicative of a greater uniformity of values for the data points within the series of data points. Thus, as is clearly seen within the series of data points of FIG. **3**, there is observed an enhanced line-to-line capacitance uniformity for a fluorosilicate glass (FSG) low dielectric constant dielectric layer formed employing the method of the present invention upon a silicon semiconductor substrate having a silicon semiconductor substrate temperature of about 410 degrees centigrade than a corresponding fluorosilicate glass (FSG) layer formed employing a method otherwise equivalent to the method of the present invention, but employing a silicon semiconductor substrate temperature of about 450 degrees centigrade rather than about 410 degrees centigrade.

As is understood by a person skilled in the art, the preferred embodiment and examples of the present invention are illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to methods, materials, structures and dimensions employed for forming a silicon containing dielectric layer in accord with the preferred embodiment and examples of the present invention while still providing a silicon containing dielectric layer in accord with the present invention, as defined by the appended claims.

What is claimed is:

1. A method for forming a dielectric layer comprising:

providing a substrate;

forming over the substrate a patterned conductor layer;

forming upon the patterned conductor layer, while employing a plasma enhanced chemical vapor deposition (PECVD), a silicon containing dielectric layer, wherein when forming the silicon containing dielectric layer there is controlled a temperature of the substrate by use of a backside cooling gas pressure so that there is enhanced a line-to-line capacitance uniformity of the patterned conductor layer.

2. The method of claim **1** wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. The method of claim **1** wherein the patterned conductor layer is selected from the group consisting of patterned conductor metal layers, patterned conductor metal alloy layers, patterned conductor polysilicon layers and patterned conductor polycide layers.

4. The method of claim **1** wherein the patterned conductor layer is formed to a thickness of from about 3000 to about 15000 angstroms.

5. The method of claim **1** wherein the plasma enhanced chemical vapor deposition (PECVD) method is selected from the group consisting of inductively coupled radio frequency plasma enhanced chemical vapor deposition (PECVD) methods, electron cyclotron resonance (ECR) plasma enhanced chemical vapor deposition (PECVD) methods and high density plasma chemical vapor deposition (HDP-CVD) methods.

6. The method of claim **1** wherein the silicon containing dielectric layer is selected from the group consisting of silicon oxide dielectric layers, silicon nitride dielectric layers, silicon oxynitride dielectric layers and fluorosilicate glass (FSG) dielectric layers.

7. The method of claim **1** wherein the silicon containing dielectric layer is formed to a thickness of from about 4000 to about 24000 angstroms.

8. The method of claim **1** wherein the temperature is controlled within a range of from about 350 to about 450 degrees centigrade.

9. The method of claim **1**, wherein the backside cooling gas is comprised of helium.

10. The method of claim 1, wherein the backside cooling gas pressure is from about 2 to 10 torr.

11. The method of claim 1, wherein the backside cooling gas pressure is from about 2 to 10 torr; the temperature of the substrate is from about 380 to 450° C.; and the silicon containing dielectric layer is comprised of FSG.

12. The method of claim 1, wherein the backside cooling gas pressure is about 4 torr; the temperature of the substrate is about 410° C.; and the silicon containing dielectric layer is comprised of FSG.

13. The method of claim 1, wherein formation of the PECVD silicon containing layer is achieved at a bias sputtering power of from about 100 to 4000 watts.

14. A method for forming a dielectric layer comprising:

providing a semiconductor substrate;

forming over the semiconductor substrate a patterned conductor layer;

forming upon the patterned conductor layer, while employing a plasma enhanced chemical vapor deposition (PECVD), a silicon containing dielectric layer, wherein when forming the silicon containing dielectric layer there is controlled a temperature of the substrate by use of a backside cooling gas pressure so that there is enhanced a line-to-line capacitance uniformity of the patterned conductor layer.

15. The method of claim 14 wherein the patterned conductor layer is selected from the group consisting of patterned conductor metal layers, patterned conductor metal alloy layers, patterned conductor polysilicon layers and patterned conductor polycide layers.

16. The method of claim 14 wherein the patterned conductor layer is formed to a thickness of from about 3000 to about 15000 angstroms.

17. The method of claim 14 wherein the plasma enhanced chemical vapor deposition (PECVD) method is selected from the group consisting of inductively coupled radio frequency plasma enhanced chemical vapor deposition (PECVD) methods, electron cyclotron resonance (ECR) plasma enhanced chemical vapor deposition (PECVD) methods and high density plasma chemical vapor deposition (HDP-CVD) methods.

18. The method of claim 14 wherein the silicon containing dielectric layer is selected from the group consisting of silicon oxide dielectric layers, silicon nitride dielectric layers, silicon oxynitride dielectric layers and fluorosilicate glass (FSG) dielectric layers.

19. The method of claim 14 wherein the silicon containing dielectric layer is formed to a thickness of from about 4000 to about 24000 angstroms.

20. The method of claim 14 wherein the temperature is controlled within a range of from about 350 to about 450 degrees centigrade.

21. The method of claim 14, wherein the backside cooling gas is comprised of helium.

22. The method of claim 14, wherein the backside helium cooling gas pressure is from about 2 to 10 torr.

23. The method of claim 14, wherein the backside helium cooling gas pressure is from about 2 to 10 torr; the temperature of the substrate is from about 380 to 450° C.; and the silicon containing dielectric layer is comprised of FSG.

24. The method of claim 14, wherein the backside helium cooling gas pressure is about 4 torr; the temperature of the substrate is about 410° C.; and the silicon containing dielectric layer is comprised of FSG.

25. The method of claim 14, wherein formation of the PECVD silicon containing layer is achieved at a bias sputtering power of from about 100 to 4000 watts.

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